Oxide-Confined Formation of Germanium Nanowire Heterostructures for High-Performance Transistors

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ABSTRACT Over the past several years, the formation of nanowire heterostructures *via* a solid-state reaction between a semiconductor nanowire and metal contact pads has attracted great interest. This is owing to its ready application in nanowire field-effect transistors (FETs) with a well-controlled channel length using a facile rapid thermal annealing process. We report the effect of oxide confinement on the formation of Ge nanowire heterostructures *via* a controlled reaction between a vapor–liquid–solid-grown, single-crystalline Ge nanowire and Ni pads. In contrast to the previous formation of Ni_2Ge/Ge/Ni_2Ge nanowire heterostructures, a segment of high-quality epitaxial NiGe was formed between Ni_2Ge and Ge with the confinement of Al_2O_3 during annealing. Significantly, back-gate FETs based on this Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge heterostructure demonstrated a high-performance p-type transistor behavior, showing a large on/off ratio of more than 10^5 and a high normalized transconductance of 2.4 $\mu S/\mu m$. The field-effect hole mobility was extracted to be 210 $cm^2/(V\ s)$. Temperature-dependent $I-V$ measurements further confirmed that NiGe has an ideal ohmic contact to p-type Ge with a small Schottky barrier height of 0.11 eV. Moreover, the hysteresis during gate bias sweeping was significantly reduced after Al_2O_3 passivation, and our Ω-gate Ge nanowire FETs using Al_2O_3 as the top-gate dielectric showed an enhanced subthreshold swing and transconductance. Therefore, we conclude that the Al_2O_3 layer can effectively passivate the Ge surface and also serve as a good gate dielectric in Ge top-gate FETs. Our innovative approach provides another freedom to control the growth of nanowire heterostructure and to further achieve high-performance nanowire transistors.

KEYWORDS: germanium nanowire heterostructure · oxide confinement · nickel germanide · atomically sharp interface · field-effect transistor

The solid-state reaction between a semiconductor nanowire and metal contacts has been long believed to produce a nanowire heterostructure with sharp and clean interfaces between the semiconductor and the formed compound.[1−8] Recently, various metal–group IV semiconductor (Si, Ge) nanowire systems have been extensively studied for exploring novel Si (Ge) nanowire heterostructures, such as NiSi,[1,3] Co_2Si/CoSi,[4] PtSi,[5] Cu_3Ge,[6] MnSi,[7] and Ni_2Ge.[8] Although the world's first transistor was made with Ge, Si replaced Ge shortly afterward and become the mainstream material in today's integrated circuit technology due to the nearly perfect interface between Si and SiO_2 (either native or thermal oxide).[9] It is also observed that the SiO_2 shell has a substantial confinement effect on the nickel silicide growth along with phase transformation in a Si nanowire.[10] Ge, as another group IV semiconductor material, has become an intriguing complement to Si due to its high electron and hole mobilities to improve complementary metal-oxide-semiconductor (CMOS) performances for further device miniaturization.[11,12] However, for Ge nanowires it has been a great challenge to produce similar heterostructures owing to the lack of high-quality GeO_x. As expected, the segregation of germanide nanoparticles was observed in the formation of germanide/Ge/germanide nanowire heterostructure during annealing.[8] Therefore, it is crucial to study the oxide confinement effect during the formation of nanowire heterostructures, especially for semiconductors without a stable native oxide, such as Ge.

In this article, we report an innovative approach to achieve high-performance Ge nanowire transistors by using Al_2O_3 to passivate the Ge surface and confine the nanowire during the formation of the Ni_xGe/Ge/Ni_xGe nanowire heterostructure. With a capping of Al_2O_3 during the rapid thermal annealing (RTA) process, the reaction product Ni_xGe maintains a perfect epitaxial relationship with Ge, providing an atomically sharp interface as well as an ideal contact to Ge. Finally, our field-effect transistors (FETs) built on this Ni_xGe/Ge/Ni_xGe heterostructure show a superior transistor

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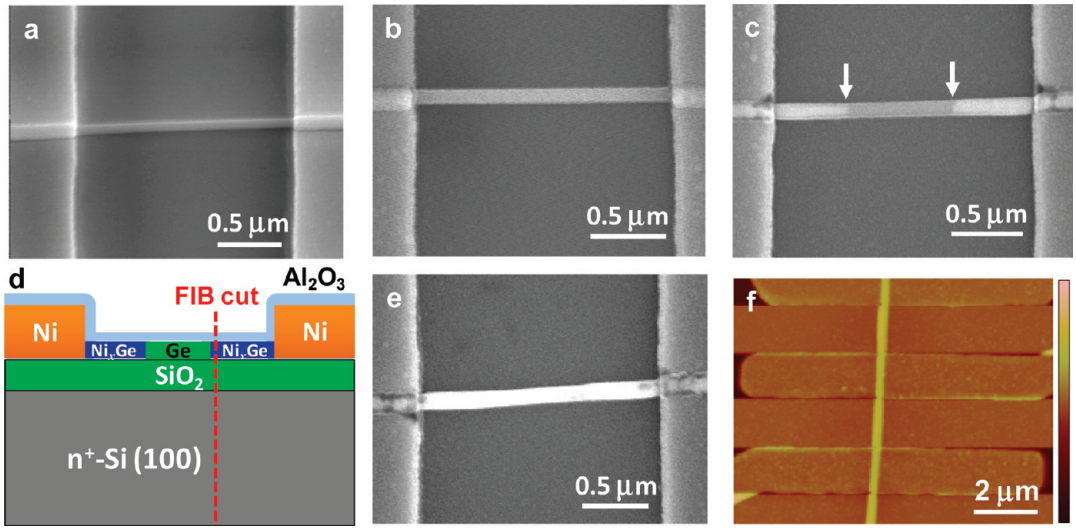

Figure 1. Formation of $Ni_xGe/Ge/Ni_xGe$ heterostructure. (a) SEM image of the as-fabricated Ge nanowire device with EBL-defined Ni electrodes. (b) SEM image of the Ge nanowire device after a conformal capping of 20 nm thick Al_2O_3. (c) SEM image of the $Ni_xGe/Ge/Ni_xGe$ heterostructure after RTA at 450 °C for 20 s in which the length of the Ge region was easily controlled to be several hundred nanometers. The arrows indicate the growth tip of the Ni_xGe nanowire. (d) Schematic illustration showing the formation of $Ni_xGe/Ge/Ni_xGe$ nanowire heterostructure with the Al_2O_3 confinement. The red line indicates the position chosen for FIB to study the cross-sectional structure in Figure 2. (e) SEM image of a fully germanided Ge nanowire. (f) AFM image of a Ge nanowire device after annealing, showing no apparent segregated nanoparticles on the surface along the nanowire.

performance compared to that from unreacted Ge nanowires.

RESULTS AND DISCUSSION

Figure 1a shows the scanning electron microscopy (SEM) image of an as-fabricated Ge nanowire device showing uniform contrast. Prior to RTA, 20 nm thick Al_2O_3 was deposited on top by atomic layer deposition (ALD) at 250 °C (Figure 1b). It was noticed that the diameter of the Ge nanowire was increased after the Al_2O_3 deposition since ALD provided a conformal coverage. After extensive experiments, this Al_2O_3 layer was found to efficiently prevent the Ge nanowire from breaking up during the annealing process and, in the meanwhile, to effectively passivate the Ge nanowire surface to minimize dangling bonds,[13,14] and finally to serve as an excellent gate dielectric for top-gate nanowire transistors.

After the Al_2O_3 deposition, the sample was then annealed with RTA in N_2 ambient to allow for the thermal intrusion of Ni into the Ge nanowire and subsequently form the Ni_xGe/Ge heterostructures along the nanowire. Clear diffusion of Ni into the Ge nanowire was observed in both SEM and transmission electron microscopy (TEM), and the formed germanide was analyzed in high-resolution TEM (HRTEM), as explained later. Figure 1c shows the SEM image of the $Ni_xGe/Ge/Ni_xGe$ heterostructures after RTA at 450 °C for 20 s. Clear contrast was observed between the Ge nanowire and the formed nickel germanide nanowire, which is attributed to the conductivity difference of the two. The remaining Ge nanowire region was easily controlled down to several hundred nanometers, and it can be further reduced to sub-50 nm.[7,8] Figure 1d schematically illustrates the formation of $Ni_xGe/Ge/Ni_xGe$ nanowire heterostructure with the Al_2O_3 confinement. The red line indicates the position where the device was cut with a focused ion beam (FIB) to study the cross-sectional structure, as explained in Figure 2. Proper control of annealing time can convert the whole Ge nanowire to a fully germanide nanowire (Figure 1e). Furthermore, atomic force microscopy (AFM) scanning showed uniform contrast without segregation of nanoparticles on the surface along the Ni_xGe/Ge heterostructure nanowire after annealing (Figure 1f), as further supported by TEM later.

Figure 2a shows the low-magnification cross-sectional TEM image of the Ni_xGe/Ge nanowire heterostructure that was cut with FIB from the nanowire FET device, as shown in Figure 1c. The $Ni_xGe/Ge/Ni_xGe$ nanowire device capped with 20 nm Al_2O_3 was fabricated on a SiO_2/Si wafer. When preparing the cross-section of Ni_xGe for TEM analysis using FIB, we chose the position as close as to the Ni_xGe/Ge interface. It is noted that in the cross-sectional view, there were some nanoparticles segregated on the SiO_2 surface from the bottom of the formed nickel germanide, which was not confined by the Al_2O_3 capping layer. This result also explains the fact that we did not observe nanoparticles on the Al_2O_3-capped surface from the AFM scanning. Figure 2b shows the lattice-resolved HRTEM image of the interface between the formed Ni_xGe nanowire and the segregated Ni_xGe nanoparticle, which were both identified to be NiGe from the fast Fourier transform (FFT, shown in the inset of Figure 2b) pattern. NiGe has an orthorhombic lattice structure with lattice constants

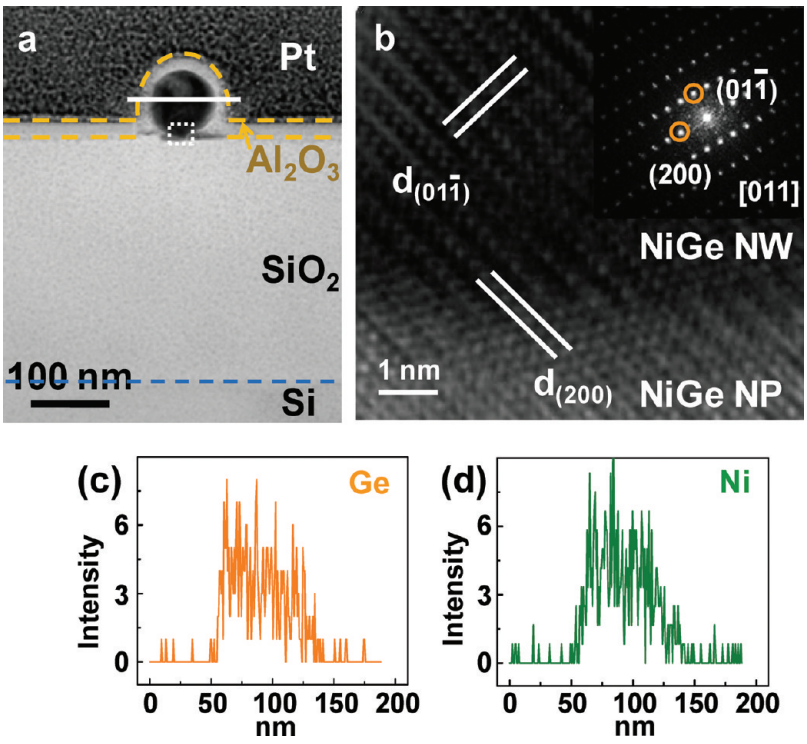

Figure 2. Cross-sectional TEM study of a Ni−Ge nanowire device on a SiO_2/Si substrate cut with FIB. (a) Low-magnification cross-sectional TEM image of the NiGe region. The 20 nm thick Al_2O_3 provides a conformal capping on the device surface, and there are germanide nanoparticles segregated underneath the nanowire, the region that is not covered by Al_2O_3. (b) Lattice-resolved HRTEM image of the interface between the formed NiGe nanowire (NW) and the segregated NiGe nanoparticle (NP), as indicated by the white rectangle in (a). The inset shows the corresponding FFT pattern. The labeled lattice spacings for NiGe are $d_{(01\bar{1})}$ = 0.295 nm and $d_{(200)}$ = 0.269 nm. (c and d) EDS line-scan profiles of Ge and Ni across the region indicated by the white line in (a), showing a Ni/Ge ratio of about 1:1.

a = 0.538 nm, *b* = 0.342 nm, and *c* = 0.581 nm (space group 62). The energy-dispersive spectrometer (EDS) line-scan results in Figures 2c and d also proved that the Ni/Ge concentration ratio is about 1:1 in the formed nickel germanide as well as in the segregated nanoparticles (the EDS line profile is not shown).

To study the epitaxial relationships between Ni_xGe and Ge, the Al_2O_3-coated Ni−Ge nanowire devices were prepared, and the TEM grids were then annealed both *in situ* and *ex-situ* (in RTA). Figure 3a shows the low-magnification TEM image of the Ni−Ge nanowire device capped with 10 nm Al_2O_3 after annealing at 450 °C for 30 s. The enlarged TEM image in Figure 3b shows that there are two interfaces in the Ni_xGe/Ge nanowire heterostructure. Figure 3c shows the EDS line-scan profile from the nanowire heterostructure. The line profile indicates two germanide phases in the formed Ni_xGe region, which corresponds to the two interfaces observed in the Ni_xGe/Ge heterostructure. The Ni/Ge ratio is about 1:1 in the small germanide region close to the Ni_xGe/Ge interface, suggesting the formation of NiGe. This result is consistent with the line-scan profile in Figure 2c and d. The length of the NiGe region can range from tens of nanometers to hundreds of nanometers in our experiments. On the other hand, the Ni/Ge ratio is about 2:1 in the other germanide region close to the Ni pad on the left, implying that the phase is Ni_2Ge. It is also worth noting that the almost constant concentration of Ge along the heterostructure suggests Ni is the dominant diffusion species in this system.[15] Figure 3d shows the lattice-resolved HRTEM image of the Ni_xGe/Ge heterostructure, clearly exhibiting two interfaces. The FFT patterns at the Ni_2Ge, NiGe, and Ge regions are shown in Figures 3e−g, which help further confirm the germanide phases. The crystallographic epitaxial relationships between the Ge/NiGe interface were determined to be Ge[01$\bar{1}$]//NiGe[010] and Ge(1$\bar{1}\bar{1}$)//NiGe(001), while those for the Ni_2Ge/NiGe interface were Ni_2Ge [100]//NiGe[010] and Ni_2Ge-(011)//NiGe(001). In contrast, the epitaxial relationships in our previously reported Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure formed without oxide confinement during annealing were found to be Ge[01$\bar{1}$]//Ni_2Ge-[0$\bar{1}$1] and Ge(1$\bar{1}\bar{1}$)//Ni_2Ge(100).[8] Therefore, the Al_2O_3 capping layer in the present study plays an important role in confining the growth of germanides and also promoting the formation of NiGe to maintain the epitaxial relationships between Ni_2Ge and Ge. Various Al_2O_3 thicknesses ranging from 5 to 20 nm were also studied to investigate the lower limit of the confining oxide thickness. (See the Supporting Information.) For both Ge nanowire heterostructures, it is worth noting that the nanowire growth direction (along the Ge [111] direction) is not perpendicular to the epitaxial planes

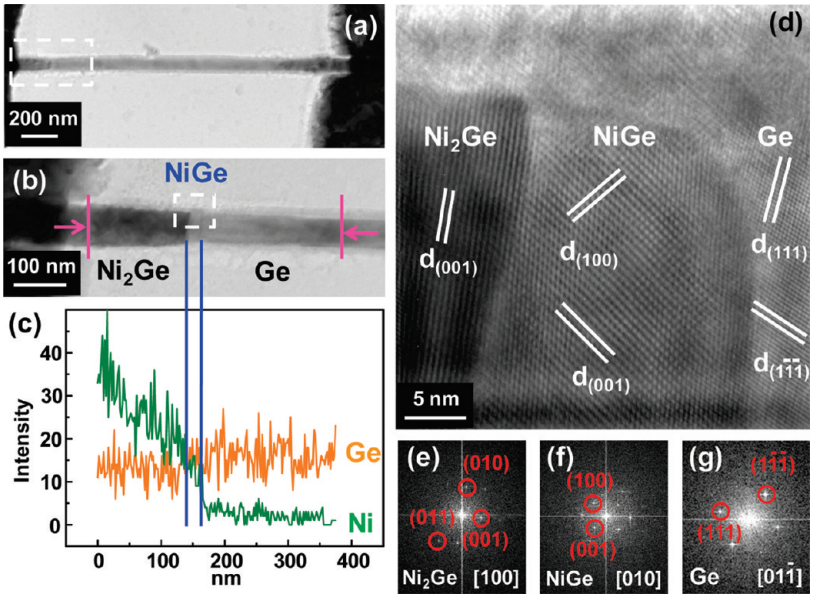

Figure 3. Plane-view TEM images of Ni−Ge nanowire devices on a TEM grid with a 50 nm thick Si_3N_4 window. (a) Low-magnification TEM image of a Ge nanowire reacted with 120 nm thick Ni pads upon 450 °C RTA for 30 s. (b) Enlarged TEM image from the white rectangle in (a). These regions with different contrasts and compositions are labeled. (c) Corresponding EDS line-scan profiles of Ge and Ni across the region between two red lines in (b). (d) Lattice-resolved TEM image of the formed Ni_xGe/Ge nanowire heterostructure from the white rectangle in (b). The labeled lattice spacings are $d_{(001)}$ = 0.5036 nm and $d_{(010)}$ = 0.3948 nm for Ni_2Ge; $d_{(100)}$ = 0.538 nm and $d_{(001)}$ = 0.5811 nm for NiGe; $d_{(111)}$ = 0.3265 nm and $d_{(1-1-1)}$ = 0.3265 nm for Ge. (e−g) FFT patterns taken from the Ni_2Ge, NiGe, and Ge regions in (d), respectively.

(parallel to the Ge (1$\bar{1}\bar{1}$) plane). This unique "twisted" growth mode is substantially different from that in typical epitaxial growth of thin films, and further microscopic studies are required to understand the growth kinetics. (See Supporting Information.)

Similar to the previous work on the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure,[8] the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure with atomically sharp interfaces can be used to explore the promising applications in nanoscale devices, such as nanowire FETs.[1,2,5,6,8] To study the electrical transport property of the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostucture, back-gated FETs were fabricated on the SiO_2/Si substrate using the degenerately doped Si as the back-gate, which provided an efficient and convenient approach to evaluate the device performance, such as the on/off ratio and carrier mobilities. In order to study the effect of Al_2O_3 capping and RTA, $I_{ds}-V_g$ curves were recorded before Al_2O_3 deposition, after Al_2O_3 deposition at 250 °C, and after RTA at 450 °C, as shown in Figure 4a. Typically as-fabricated devices show a p-type transistor behavior with an on/off ratio in the range $10-10^2$ before Al_2O_3 deposition. The typical on current is about 10−100 nA at a drain bias of V_{ds} = 0.1 V. The Ni contact to the Ge nanowire is improved after Al_2O_3 deposition, and the on/off ratio is enhanced to above 10^3. Further RTA at 450 °C for 20 s can significantly raise the on/off ratio up to $>10^5$ owing to the formation of single-crystalline NiGe in which a perfect contact to the Ge channel is developed with reduced contact resistance. Also, the subthreshold swing is calculated to decrease from 4.49 V/dec to 1.74 V/dec after RTA at 450 °C for our back-gate Ge nanowire FETs. To extract the field-effect hole mobilities before and after RTA, we first used the cylinder-on-plate model to estimate the gate capacitance coupling between the Ge nanowire and the back-gate oxide as[16]

$$C_{ox} = \frac{2\pi\varepsilon_{ox}\varepsilon_0 L}{\cosh^{-1}\left(\frac{r+t_{ox}}{r}\right)}$$

where $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm is the vacuum dielectric constant, ε_{ox} = 3.9 is the relative dielectric constant for SiO_2, and r = 35 nm is the radius of the Ge nanowire. The Ge nanowire channel before and after RTA has a length of L = 1.9 μm and L = 0.67 μm, respectively; the thickness of the back-gate dielectric is t_{ox} = 330 nm. Given the above parameters, the estimated gate capacitance is $C_{ox} = 1.36 \times 10^{-16}$ F and $C_{ox} = 4.79 \times 10^{-17}$ F, before and after RTA, respectively. The field-effect hole mobility can be extracted from $I_{ds}-V_g$ curves using the transconductance (g_m) at a fixed drain bias V_{ds}:

$$\mu = \frac{g_m L^2}{V_{ds} C_{ox}}$$

Using the maximum transconductance extracted from $I_{ds}-V_g$ curves, the hole mobility is calculated to be 210 and 94.2 cm^2/V s, before and after RTA, respectively. The improvement in the hole mobility is also attributed to the improvement in source/drain contact after annealing.

Dual sweepings of gate bias in $I_{ds}-V_g$ curves were performed to study the impact of the Al_2O_3 capping

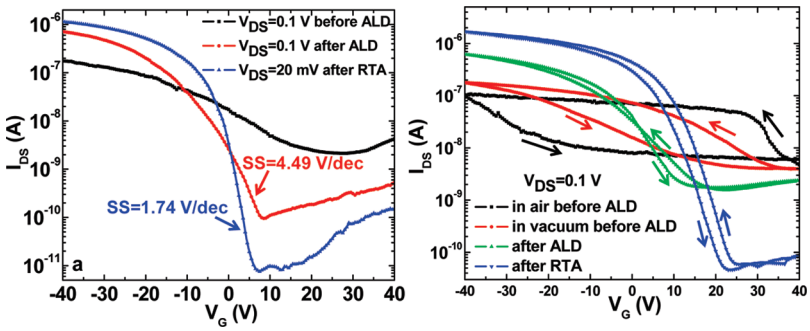

Figure 4. Electrical characterization on the effects of ALD-Al_2O_3 deposition and RTA. (a) $I_{ds}-V_g$ curves of a back-gate Ge nanowire transistor recorded before ALD, after ALD at 250 °C, and after RTA at 450 °C, all showing a p-type transistor behavior. The back-gate transistor after RTA at 450 °C for 20 s shows an on/off ratio of more than 10^5 and an extracted field-effect hole mobility of 210 $cm^2/(V\ s)$. (b) Dual sweepings of the gate bias V_g between +40 and −40 V showing different sizes of hysteresis under various conditions. The arrows indicate the sweeping directions. The hysteresis was significantly reduced after the Al_2O_3 passivation. Small hysteresis was still observed after RTA, which may be attributed to the charge trapping on the Ge surface between the Ge nanowire channel and the back-gate dielectric, the region that is not covered by the Al_2O_3 capping layer.

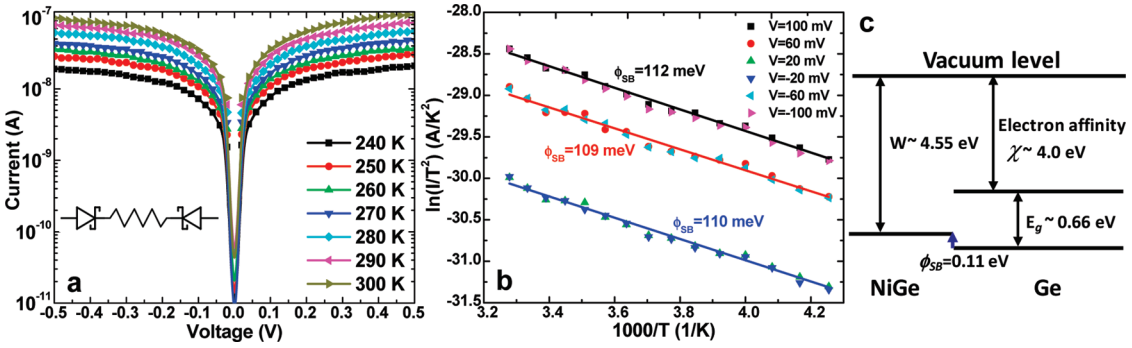

Figure 5. Temperature-dependent characterization of the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure. (a) $I-V$ measurements of the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure at temperatures ranging from 240 to 300 K. The inset shows the corresponding circuit symbol. (b) Arrehenius plot for the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure at various biases between 235 and 305 K. The extracted Schottky barrier height of NiGe to Ge is about 0.11 eV. (c) Corresponding band structure diagram of the NiGe/Ge contact.

layer on passivating the Ge nanowire surface. Figure 4b shows the $I_{ds}-V_g$ curves recorded under various conditions: before Al_2O_3 deposition (both in air and in vacuum), after Al_2O_3 deposition at 250 °C, and after RTA at 450 °C. The gate bias was swept from +40 V to −40 V then back to +40 V in steps of 0.5 V at a fixed drain bias of V_{ds} = 0.1 V. The $I_{ds}-V_g$ curve measured in air before annealing shows the biggest hysteresis, which is mainly due to the absorption of molecules from the ambient and the charge trapping on the Ge surface.[17,18] The measured reduced hysteresis in a vacuum (less than 10^{-5} Torr), however, rules out the contribution from the ambient. Furthermore, the hysteresis was significantly reduced after the Al_2O_3 deposition, which unambiguously demonstrates the passivation effect of the Al_2O_3 layer on the Ge nanowire surface.[19] The small hysteresis present after Al_2O_3 passivation and after RTA, however, may arise from the charge trapping on the Ge surface between the Ge nanowire channel and the back-gate dielectric, the region that is not covered by the Al_2O_3 capping layer.

Although we intended to grow undoped Ge nanowires, their performance as nanowire transistors usually shows a p-type behavior in nature, which is mainly due to the surface state-induced Fermi level pinning that results in hole accumulation.[17,20] Temperature-dependent $I-V$ measurements were performed to extract the Schottky barrier height of the formed NiGe contact to the Ge nanowire. Figure 5a shows the two-terminal $I-V$ measurements at various temperatures after RTA at 450 °C for 20 s, illustrating a back-to-back Schottky diode behavior. Figure 5b shows the Arrehenius plot for the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure at various biases between 235 and 305 K.[6,7] The linear fitting of $\ln(I/T^2)$ *versus* $1/T$ gave a Schottky barrier height of 0.11 eV. The consistent behaviors under positive and negative biases demonstrate symmetric source/drain contacts. Measurements over several batches gave a barrier height in the range 0.11−0.13 eV. The corresponding band diagram shows an ohmic contact to a p-type Ge nanowire and a Schottky contact to an n-type Ge nanowire with a barrier height about 0.55 eV.

The characteristics of the back-gate Ge nanowire FETs were shown in Figure 6. Figure 6a shows the SEM image of a back-gate FET with multiple Ni probes fabricated on a SiO_2/Si substrate. Clear diffusion of Ni into the Ge nanowire was observed for each Ni

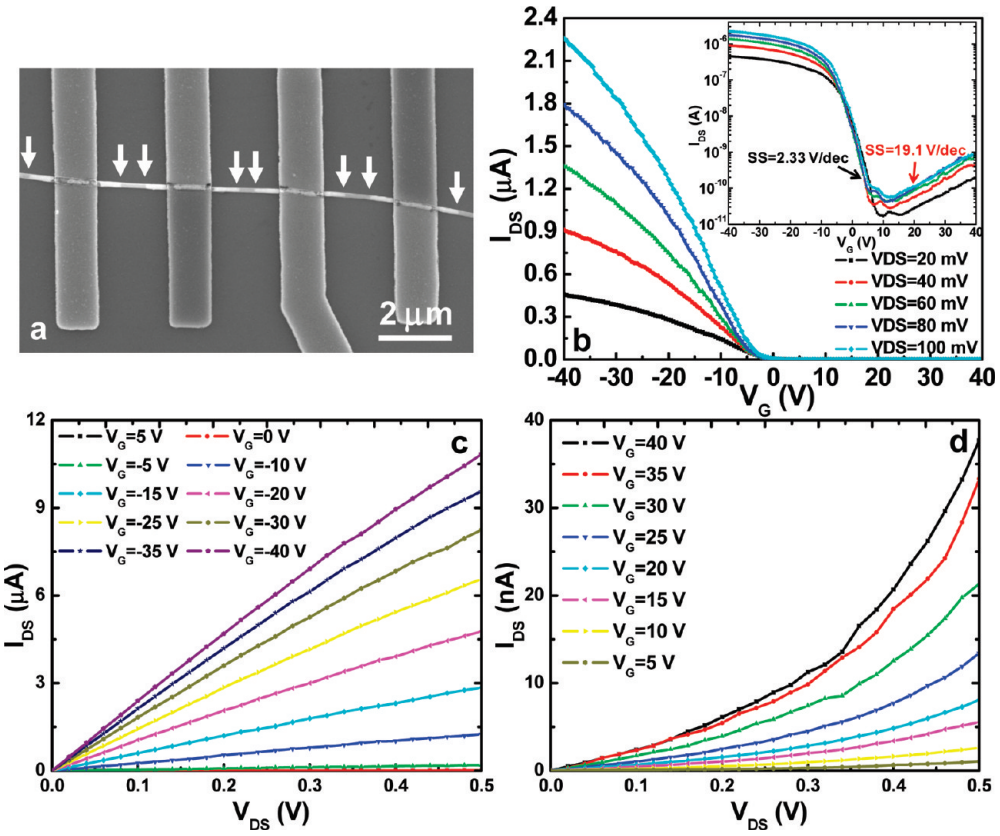

Figure 6. Back-gate Ge nanowire FET characterization. (a) SEM image of a back-gate FET with multiple Ni probes. The arrows highlight the growth tip of the Ni_2Ge/NiGe nanowire. (b) $I_{ds}-V_g$ curves of the back-gate Ge nanowire transistor after RTA at 450 °C for 20 s, showing an electron-conduction part ($V_g > 10$ V) and a hole-conduction part ($V_g < 10$ V) at different gate biases. (c) $I_{ds}-V_{ds}$ curves of the hole-conduction part, showing an ohmic behavior. (d) $I_{ds}-V_{ds}$ curves of the electron-conduction part, showing a Schottky behavior.

electrode, and the process has a high yield after RTA with an Al_2O_3 capping. Figure 6b shows the typical $I_{ds}-V_g$ curves of a back-gate Ge nanowire FET, and the inset gives a logarithmic plot of drain current I_{ds} *versus* gate voltage V_g relations at various drain voltages. The maximum transconductance is obtained as about 0.168 μS at $V_{ds} = 0.1$ V, which gives rise to a normalized transconductance of 2.4 μS/μm, assuming the effective channel length is equal to the nanowire diameter (70 nm).[5] The extracted hole mobility in our experiments is typically in the range 150−210 cm^2/(V s). An apparent transition from electron conduction ($V_g > 10$ V) to hole conduction ($V_g < 10$ V) was observed. The subthreshold swing is extracted to be 19.1 and 2.33 V/dec for electron conduction and hole conduction, respectively. The smaller conduction current and the larger subthreshold swing for the electron-conduction region is due to a larger Schottky barrier for electrons (~0.55 eV) compared with that for holes (~0.11 eV). Figure 6c and d show the $I_{ds}-V_{ds}$ curves for the hole conduction and electron conduction, respectively. The different characteristics further support NiGe as an ohmic contact to *p*-type Ge (linear $I_{ds}-V_{ds}$ characteristics at small V_{ds}) and a Schottky contact to n-type Ge (highly nonlinear $I_{ds}-V_{ds}$ characteristics). Saturation behavior in the $I_{ds}-V_{ds}$ characteristics for the hole conduction can be observed at large V_{ds}. (See the Supporting Information.)

As mentioned before, the Al_2O_3 capping layer can also be used as a top-gate dielectric to build Ω-gate transistors on the formed Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure. Figure 7a schematically illustrates the device structure of a Ge nanowire FET with both back-gate and top-gate contacts. Figure 7b shows the SEM image of a top-gate transistor, in which the Ti/Au gate metal was deposited by e-beam evaporation. In order to reduce the gate leakage current through the overlap between the gate and the formed Ni_xGe region, another layer of Al_2O_3 was deposited with ALD on top of the Al_2O_3-capped Ge nanowire device before the gate metal deposition. The total thickness of the Al_2O_3 layer is 23 nm, and its relative dielectric constant is extracted to be 7.5 from the calibrating capacitance−voltage ($C-V$) measurements. Figure 7c shows the $I_{ds}-V_g$ curves of a back-gate Ge nanowire transistor, giving a subthreshold swing of 3.44 V/dec and a maximum normalized transconductance of 1.39 μS/μm at $V_{ds} = 0.2$ V. In comparison, Figure 7d shows the $I_{ds}-V_g$ curves of the Ω-gate Ge nanowire transistor fabricated after passivation, showing a

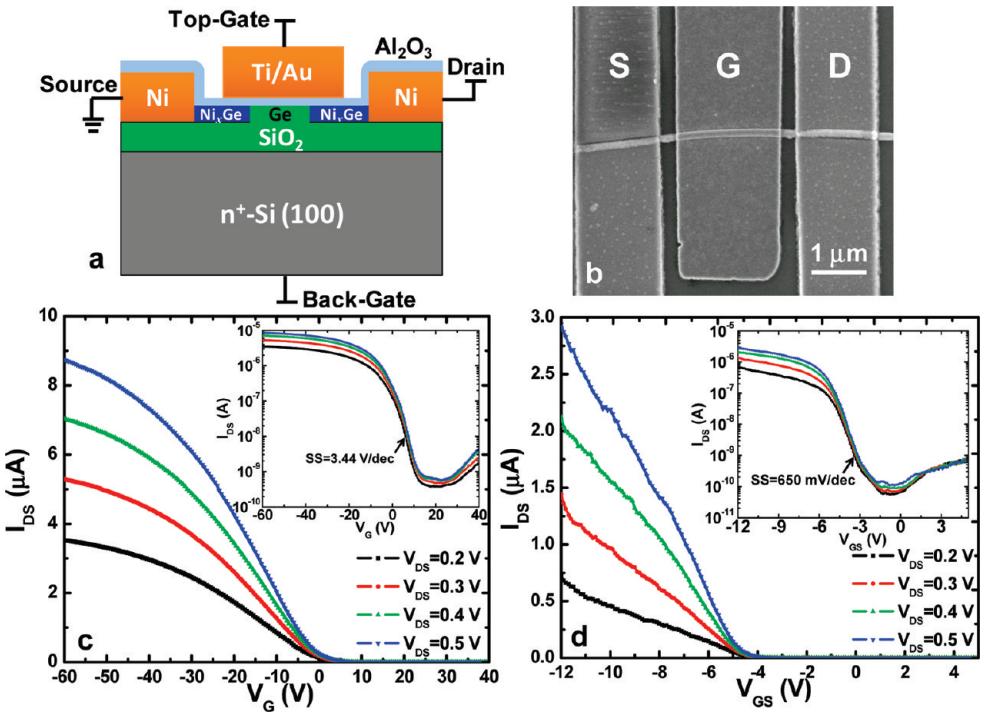

Figure 7. Comparison of back-gate and top-gate Ge nanowire FETs. (a) Schematic illustration of a Ge nanowire FET with both back-gate contact and top-gate contacts. (b) SEM image of a top-gate FET device. (c) $I_{ds}-V_g$ curves of the back-gate Ge nanowire transistor with a poor subthreshold swing of 3.44 V/dec. The inset shows the logarithm plot of $I_{ds}-V_g$ curves. (d) $I_{ds}-V_g$ curves of the top-gate Ge nanowire transistor, showing an improved subthreshold swing of 650 mV/dec. The inset shows the logarithm plot of $I_{ds}-V_g$ curves.

subthreshold swing of 650 mV/dec and a maximum transconductance of 3.27 μS/μm at $V_{ds} = 0.2$ V. Also, the typical field-effect hole mobility in the top-gated transistors falls in the range 100–150 cm^2/(V s). The improvement in the subthreshold swing and transconductance can be attributed to the increment in gate capacitance and the enhancement of gate control over the nanowire channel in the top-gated device, while the degradation of hole mobility is due to additional scatterings from the top-gate dielectric/Ge nanowire channel interface.[21,22]

CONCLUSIONS

In summary, a Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure with atomically sharp interfaces has been formed by the thermal intrusion of Ni into a Ge nanowire at 450 °C. A segment of NiGe was formed between Ni_2Ge and Ge with an Al_2O_3 capping during annealing. The Al_2O_3 capping provided appreciable confinement during the growth of germanide and changes its composition to maintain the epitaxial relationships. In addition, the Al_2O_3 layer also helped to prevent nanowire breaking and passivate the Ge nanowire surface. SEM and TEM studies showed a well-controlled diffusion process, in which the remaining Ge region was easily controlled down to hundreds of nanometers by RTA. Back-gate FETs were fabricated using the formed Ni_2Ge/NiGe heterostructure as source/drain contacts to the Ge nanowire channel. The electrical measurement showed a high-performance p-type behavior with an on/off ratio of more than 10^5, a maximum transconductance of 2.4 μS/μm, and a field-effect hole mobility of 210 cm^2/(V s). The Schottky barrier height extracted from temperature-dependent $I-V$ measurements was about 0.11 eV, which affirmed that NiGe was a good Ohmic contact to p-type Ge nanowires. Moreover, our Ω-gate Ge nanowire transistors using the Al_2O_3 layer as the gate dielectric further improved the subthreshold swing and transconductance.

EXPERIMENTAL METHODS

Device Fabrication. Single-crystalline Ge nanowires with ⟨111⟩ growth direction were synthesized vertically on a SiO_2/Si(100) wafer using a conventional vapor–liquid–solid (VLS) method, as described elsewhere.[23] Briefly, a 0.5 nm thick Au film, which served as the catalytic layer, was thermally evaporated on the SiO_2/Si(100) substrate. Then the substrate was annealed at 270–320 °C with a pressure of 10 Torr in the ambient of GeH_4 (12 sccm, 10% balanced in H_2), which is the precursor gas for Ge nanowire growth. The VLS-grown Ge nanowires are typically 70–80 nm in diameter with lengths over 10 μm. Ge nanowires are not doped on purpose during growth, but unintentional doping usually occurs.[20,24] In order to enhance the quantum confinements, Ge nanowires with smaller diameters down to sub-10 nm can be synthesized by tuning the size of the

catalyst.[25] However, it is worth noting that the shrinking of the Ge nanowire diameter is accompanied by the reduction of the melting point of the Ge nanowires.[26]

To form metal germanide/Ge nanowire heterostructures, Ge nanowires were transferred onto a SiO_2/Si substrate. The top thermal SiO_2 was about 330 nm thick. The Si substrate was heavily doped with a resistivity of 1−5 mΩ-cm, which serves as a back-gate for further device characterization. e-Beam lithography (EBL) was used to define Ni contacts to Ge nanowires. Before e-beam evaporation of Ni (with a purity of 99.995% and in a vacuum at a pressure lower than 10^{-6} Torr), the sample was dipped into diluted hydrofluoric acid for 15 s to completely remove native oxide in the contact region.

To prepare the TEM samples, VLS-grown Ge nanowires were dispersed on the TEM grids with a square opening of a Si_3N_4 thin film. The low-stress Si_3N_4 film was deposited by low-pressure chemical vapor deposition. The thickness was about 50 nm to ensure it is transparent to the electron beam without interference with images of the nanowires. Then the Ni contacts to the Ge nanowires were defined by EBL followed by e-beam evaporation. An Al_2O_3 film was deposited by ALD at 250 °C to cap the device and confine the solid-state reaction of germanidation during annealing. The Al_2O_3-coated devices were then annealed both *in situ* and *ex-situ* (in RTA). For *in situ* annealing, the samples were heated inside a TEM with a heating holder (Gatan 652 double tilt heating holder) under a RTA mode with a pressure below 10^{-6} Torr.

Characterization Methods. The Ni−Ge nanowire devices were characterized using SEM and AFM to check the surface morphology before and after annealing. A field-emission TEM (JEM-3000F, operated at 300 kV with a point-to-point resolution of 0.17 nm) equipped with an EDS was used to obtain the epitaxial relationships and determine the chemical compositions of the nanowire heterostructure. Electrical measurements were performed using a homemade probe station connected to a Keithley 4200 semiconductor parameter analyzer.

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Supporting Information Available: TEM images of Ni−Ge nanowire devices upon annealing with various confining oxide thicknesses. $I_{ds}-V_{ds}$ characteristics for a Ni−Ge nanowire device showing the saturation behavior at large V_{ds}. Schematic illustration of the epitaxial relationships of the Ni_2Ge/Ge interface in the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure and the NiGe/Ge interface in the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure. This material is available free of charge *via* the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

1. Wu, Y.; Xiang, J.; Yang, C.; Lu, W.; Lieber, C. M. Single-Crystal Metallic Nanowires and Metal/Semiconductor Nanowire Heterostructures. *Nature* **2004**, *430*, 61–65.
2. Weber, W. M.; Geelhaar, L.; Graham, A. P.; Unger, E.; Duesberg, G. S.; Liebau, M.; Pamler, W.; Chèze, C.; Riechert, H.; Lugli, P.; *et al.* Silicon-Nanowire Transistors with Intruded Nickel-Silicide Contacts. *Nano Lett.* **2006**, *6*, 2660–2666.
3. Lu, K.-C.; Wu, W.-W.; Wu, H.-W.; Tanner, C. M.; Chang, J. P.; Chen, L. J.; Tu, K. N. In situ Control of Atomic-Scale Si Layer with Huge Strain in the Nanoheterostructure NiSi/Si/NiSi through Point Contact Reaction. *Nano Lett.* **2007**, *7*, 2389–2394.
4. Chou, Y.-C.; Wu, W.-W.; Cheng, S.-L.; Yoo, B.-Y.; Myung, N.; Chen, L. J.; Tu, K. N. In situ TEM Observation of Repeating Events of Nucleation in Epitaxial Growth of Nano $CoSi_2$ in Nanowires of Si. *Nano Lett.* **2008**, *8*, 2194–2199.
5. Lin, Y.-C.; Lu, K.-C.; Wu, W.-W.; Bai, J.; Chen, L. J.; Tu, K. N.; Huang, Y. Single Crystalline PtSi Nanowires, PtSi/Si/PtSi Nanowire Heterostructures, and Nanodevices. *Nano Lett.* **2008**, *8*, 913–918.
6. Burchhart, T.; Lugstein, A.; Hyun, Y. J.; Hochleitner, G.; Bertagnolli, E. Atomic Scale Alignment of Copper-Germanide Contacts for Ge Nanowire Metal Oxide Field Effect Transistors. *Nano Lett.* **2009**, *9*, 3739–3742.
7. Lin, Y.-C.; Chen, Y.; Shailos, A.; Huang, Y. Detection of Spin Polarized Carrier in Silicon Nanowire with Single Crystal MnSi as Magnetic Contacts. *Nano Lett.* **2010**, *10*, 2281–2287.
8. Tang, J.; Wang, C.-Y; Xiu, F.; Hong, A.; Chen, S.; Wang, M.; Zeng, C.; Yang, H.-J; Tuan, H.-Y; Tsai, C.-J.; *et al.* Single-Crystalline Ni_2Ge/Ge/Ni_2Ge Nanowire Heterostructure Transistors. *Nanotechnology* **2010**, *21*, 505704.
9. Shockley, W. The Path to the Conception of the Junction Transistor. *IEEE Trans. Electron Devices* **1976**, *23*, 597–620.
10. Lin, Y.-C.; Chen, Y.; Xu, D.; Huang, Y. Growth of Nickel Silicides in Si and Si/SiO_x Core/Shell Nanowires. *Nano Lett.* **2010**, *10*, 4721–4726.
11. Wang, D.; Wang, Q.; Javey, A.; Tu, R.; Dai, H.; Kim, H.; McIntyre, P. C.; Krishnamohan, T.; Saraswat, K. C. Germanium Nanowire Field-Effect Transistors with SiO_2 and High-κ HfO_2 Gate Dielectrics. *Appl. Phys. Lett.* **2003**, *83*, 2432–2434.
12. van der Meulen, M. I.; Petkov, N.; Morris, M. A.; Kazakova, O.; Han, X.; Wang, K. L.; Jacob, A. P.; Holmes, J. D. Single Crystalline $Ge_{1-x}Mn_x$ Nanowires as Building Blocks for Nanoelectronics. *Nano Lett.* **2009**, *9*, 50–56.
13. Lamagna, L.; Fusi, M.; Spiga, S.; Fanciulli, M.; Brammertz, G.; Merckling, C.; Meuris, M.; Molle, A. Effects of Surface Passivation during Atomic Layer Deposition of Al_2O_3 on $In_{0.53}Ga_{0.47}As$ Substrates. *Microelectron. Eng.* **2011**, *88*, 431–434.
14. Bellenger, F.; Merckling, C.; Penaud, J.; Houssa, M.; Caymax, M.; Meuris, M.; Meyer, K. D.; Heyns, M. M. Interface Properties Improvement of Ge/Al_2O_3 and Ge/GeO_2/Al_2O_3 Gate Stacks using Molecular Beam Deposition. *ECS Trans.* **2008**, *16*, 411–422.
15. Hsieh, Y. F.; Chen, L. J.; Marshall, E. D.; Lau, S. S. Partial Epitaxial Growth of Ni_2Ge and NiGe on Ge(111). *Thin Solid Films* **1988**, *162*, 287–294.
16. Ramo, S.; Whinnery, J. R.; Duzer, T. V. *Fields and Waves in Communication Electronics*, 3rd ed.; Wiley: New York, 1994.
17. Hanrath, T.; Korgel, B. A. Influence of Surface States on Electron Transport through Intrinsic Ge Nanowires. *J. Phys. Chem. B* **2005**, *109*, 5518–5524.
18. Wang, D.; Chang, Y.-L.; Wang, Q.; Cao, J.; Farmer, D. B.; Gordon, R. G.; Dai, H. Surface Chemistry and Electrical Properties of Germanium Nanowires. *J. Am. Chem. Soc.* **2004**, *126*, 11602–11611.
19. Zhou, Y.; Ogawa, M.; Han, X.; Wang, K. L. Alleviation of Fermi-level Pinning Effect on Metal/Germanium Interface by Insertion of an Ultrathin Aluminum Oxide. *Appl. Phys. Lett.* **2008**, *93*, 202105.
20. Zhang, S.; Hemesath, E. R.; Perea, D. E.; Wijaya, E.; Lensch-Falk, J. L.; Lauhon, L. J. Relative Influence of Surface States and Bulk Impurities on the Electrical Properties of Ge Nanowires. *Nano Lett.* **2009**, *9*, 3268–3274.
21. Wu, M.; Alivov, Y.; Morkoç, H. High-κ Dielectrics and Advanced Channel Concepts for Si MOSFET. *J. Mater. Sci. Mater. Electron.* **2008**, *19*, 915–951.
22. Torii, K.; Shimamoto, Y.; Saito, S.; Tonomura, O.; Hiratani, M.; Manabe, Y.; Caymax, M.; Maes, J. W. The Mechanism of Mobility Degradation in MISFETs with Al_2O_3 Gate Dielectric. *VLSI Tech. Dig.* **2002**, 188–189.
23. Chueh, Y.-L.; Boswell, C. N.; Yuan, C.-W.; Shin, S. J.; Takei, K.; Ho, J. C.; Ko, H.; Fan, Z.; Haller, E. E.; Chrzan, D. C.; *et al.* Nanoscale Structural Engineering *via* Phase Segregation: Au-Ge System. *Nano Lett.* **2009**, *10*, 393–397.
24. Zhang, L.; Tu, R.; Dai, H. Parallel Core-Shell Metal-Dielectric-Semiconductor Germanium Nanowires for High-Current Surround-Gate Field-Effect Transistors. *Nano Lett.* **2006**, *6*, 2785–2789.
25. Greytak, A. B.; Lauhon, L. J.; Gudiksen, M. S.; Lieber, C. M. Growth and Transport Properties of Complementary Germanium Nanowire Field-Effect Transistors. *Appl. Phys. Lett.* **2004**, *84*, 4176–4178.
26. Wu, Y.; Yang, P. Melting and Welding Semiconductor Nanowires in Nanotubes. *Adv. Mater.* **2001**, *13*, 520–523.